AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A phase frequency detector comprising:

a phase error detecting unit for outputting at least a phase error signal according to a phase error between a first input signal and a second input signal; and

a reset unit coupled to the phase error detecting unit for receiving the first input signal and the second input signal, and for outputting a reset signal according to the first input signal and the second input signal, in order to reset the phase error detecting unit;

wherein the length of the phase error signal has a substantial linear relationship with the phase error of the first input signal and the second input signal;

wherein the phase error detecting unit is reset by the reset signal responsive to an edge of the first input signal, and remains reset for a significant period of time despite of the level of the first input signal after said edge.

2. (Original) The phase frequency detector according to claim 1, wherein the phase error signal comprises a first output signal and a second output signal.

3. (Original) The phase frequency detector according to claim 1, wherein the phase error detecting unit comprises:

a first flip-flop for outputting a first flag signal according to the first input signal; and

a second flip-flop for outputting a second flag signal according to the second input signal.

4. (Original) The phase frequency detector according to claim 3, wherein the phase error detecting unit further comprises:

a sampling circuit for outputting the phase error signal according to the first flag signal and the second flag signal.

5. (Currently Amended) The phase error detector according to claim 3, wherein the ~~delay~~ time from a state transition of the first input signal to ~~the~~ a corresponding reset of the phase error detecting unit is substantially the same as the ~~delay~~ time from the state transition of the first input signal to a corresponding state transition of the first flag signal.

6. (Original) The phase frequency detector according to claim 3, wherein the reset signals signal comprises:

a first reset signal for resetting the first flip-flop; and

a second reset signal for resetting the second flip-flop.

7. (Original) The phase frequency detector according to claim 6, wherein the reset unit comprises:

a third flip-flop for outputting the second reset signal according to the first input signal; and

a fourth flip-flop for outputting the first reset signal according to the second input signal.

8. (Original) The phase frequency detector according to claim 1, wherein the phase error detecting unit further comprises a buffer circuit for buffering the first input signal and the second input signal.

9. (Cancelled)

10. (Currently Amended) A phase locked loop comprising:

a phase error detector for receiving a first input signal and a second input signal, and outputting a phase error signal; and

a clock signal generator for outputting the second input signal according to the phase error signal;

wherein the phase error detector comprises:

a phase error detecting unit for outputting the phase error signal according to a phase error between the first input signal and the second input signal; and

a reset unit coupled to the phase error detecting unit for receiving the first input signal and the second input signal, and for outputting a reset signal according to the first input signal and the second input signal, in order to reset the phase error detecting unit;

wherein the length of the phase error signal has a substantial linear relationship with the phase error of the first input signal and the second input signal.

11. (Cancelled)

12. (Original) The phase locked loop according to claim 10, wherein the clock signal generator comprises:

a phase error quantizer for receiving the phase error signal;

a digital controlled oscillator coupled to the phase error quantizer; and

a frequency divider coupled to the digital controlled oscillator.

13. (Original) The phase locked loop according to claim 10, wherein the clock signal generator comprises:

a charge pump for receiving the phase error signal;

a voltage controlled oscillator coupled to the charge pump; and

a frequency divider coupled to the voltage controlled oscillator.